

What is claimed:

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1 1. A semiconductor device comprising a field effect transistor, the field effect
2 transistor including a gate dielectric layer, a source region and a drain region, wherein a first
3 semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain
4 region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer
5 and the source region, a first offset impurity layer is provided below the first semi-recessed
6 LOCOS layer, and a second offset impurity layer is provided below the second semi-
7 recessed LOCOS layer.

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1 2. A semiconductor device according to claim 1, wherein the first semi-recessed
2 LOCOS layer and the second semi-recessed LOCOS layer each have a thickness of 0.3 – 0.7
3 μm .

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2 3. A semiconductor device according to claim 1, further comprising an element
isolation region, wherein the element isolation region has a semi-recessed LOCOS structure.

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2 4. A semiconductor device according to claim 3, wherein a channel stopper
layer is provided below the element isolation region.

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2 5. A semiconductor device according to claim 1, wherein a low concentration
impurity layer having a conductivity type identical with conductivity type of the drain region
3 is provided adjacent to the drain region.

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1 6. A method for manufacturing a semiconductor device comprising a field
2 effect transistor, the field effect transistor including a gate dielectric layer, a source region
3 and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate
4 dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided
5 between the gate dielectric layer and the source region, a first offset impurity layer is
6 provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is
7 provided below the second semi-recessed LOCOS layer, the method comprising:
8 forming a first recessed section in a region where the first semi-recessed LOCOS
9 layer is to be formed, and forming a second recessed section in a region where the second
10 semi-recessed LOCOS layer is to be formed
11 implanting an impurity in a semiconductor substrate in the first recessed section and
12 in the second recessed section; and
13 thermally oxidizing the semiconductor substrate to form the first semi-recessed
14 LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS
15 layer in the second recessed section.

1 7. A method for manufacturing a semiconductor device according to claim 6,
2 further comprising forming an anti-oxidation layer having a predetermined pattern, wherein
3 the thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS
4 layer in the first recessed section and to form the second semi-recessed LOCOS layer in the
5 second recessed section is conducted using the anti-oxidation layer formed on the
6 semiconductor substrate as a mask.

1 8. A method for manufacturing a semiconductor device according to claim 7,
2 wherein the anti-oxidation layer has a film thickness of 50 – 70 nm.

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1 9. A method for manufacturing a semiconductor device according to claim 7,
2 further comprising, before the forming of the anti-oxidation layer, forming a protection film
3 over the semiconductor substrate in the first recessed section and in the second recessed
4 section.

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1 10. A method for manufacturing a semiconductor device according to claim 9,
2 wherein the protection film is a silicon oxide layer.

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1 11. A method for manufacturing a semiconductor device according to claim 10,
2 wherein the silicon oxide layer is formed by a thermal oxidation method.

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1 12. A method for manufacturing a semiconductor device according to claim 9,
2 further comprising, after the implanting an impurity in the semiconductor substrate in the
3 first recessed section and in the second recessed section, removing the protection film.

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1 13. A method for manufacturing a semiconductor device according to claim 6,
2 wherein the first recessed section and the second recessed section each are formed in a
3 tapered configuration.

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1 14. A method for manufacturing a semiconductor device according to claim 13,
2 wherein a tapered angle of each of the first recessed section and the second recessed section
3 is 60 degrees or greater less than 90 degrees.

1 15. A method for manufacturing a semiconductor device according to claim 6,
2 wherein an implanting direction of the impurity traverses a normal line of a surface of the
3 semiconductor substrate during the implanting an impurity in the semiconductor substrate in
4 the first recessed section and in the second recessed section.

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1 16. A method for manufacturing a semiconductor device according to claim 15,
2 wherein the implanting direction of the impurity and the normal line of the surface of the
3 semiconductor substrate define an angle that is greater than zero degrees and no greater than
4 45 degrees.

1 17. A semiconductor device comprising:
2 first and second field effect transistors each including a gate dielectric layer; source
3 and drain regions; a first semi-recessed LOCOS layer positioned between the gate dielectric
4 layer and the drain region; a second semi-recessed LOCOS layer positioned between the
5 gate dielectric layer and the source region; a first offset impurity layer below the first semi-
6 recessed LOCOS layer; and a second offset impurity layer below the second semi-recessed
7 LOCOS layer; and
8 an element isolation region located between the first and second field effect
9 transistors.

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1 18. A semiconductor device according to claim 17, wherein said element
2 isolation region includes a semi-recessed LOCOS structure.

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1 19. A semiconductor device according to claim 17, further comprising a channel
2 stopper layer formed below the element isolation region.

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1 20. A liquid crystal display driver comprising the semiconductor device of claim
2 17.

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